REMARKS

Claims 1-3 and 5-33 are pending in this application, of which 7-11 and 14-28 were withdrawn from consideration. Claims 1-3, 5, 6 and 13 were rejected under 35 U.S.C. §102(b) as being anticipated by Dickirson. Claims 12 and 29-33 were rejected under 35 U.S.C. §102(e) as being anticipated by Khandros. Claims 1 and 12 are currently amended. Reconsideration is respectfully requested.

Claim 1 as currently amended distinguishes Dickirson because shielding is disposed around the signal trace. As described in the Specification at page 8, lines 5-17, and illustrated in Figure 9, the inner layer trace may be shielded between ground planes disposed on parallel layers of the circuit board. Further, vertically oriented plating may be used to interconnect the ground planes, thereby producing a coaxial-like shielding structure. The Dickirson technique fails to teach use of shielding in any form. Further, Dickirson fails to suggest any motivation to use shielding because the motivation for the Dickirson technique is to avoid volume, cost, complexity and labor costs associated with interconnecting circuits (see Col. 1, line 65 through Col. 2, line 7). In contrast, the current specification at page 2, lines 1-4 describes how cross-talk is problematic for high-frequency signals. It will be appreciated that mitigating cross-talk is one motivation for shielding the signal trace. Withdrawal of the rejection of claim 1 is therefore requested. Claims 2, 3, 5, 6 and 13 are dependent claims which further distinguish the invention, and which are allowable for the same reason as claim 1. Withdrawal of the rejections of claims 2, 3, 5, 6 and 13 is therefore requested.

Claim 12 as currently amended distinguishes Khandros because shielding is disposed around the signal trace. Again, as described in the Specification at page 8, lines 5-17, and illustrated in Figure 9, the inner layer trace may be shielded between ground planes disposed on

parallel layers of the circuit board. Further, vertically oriented plating may be used to interconnect the ground planes, thereby producing a coaxial-like shielding structure. The Khandros technique fails to teach use of shielding. Hence, claim 12 distinguishes Khandros by reciting "shielding disposed around the at least one signal trace." Further, the Khandros technique fails to even suggest direct connection of signal traces. For example, Figure 33 which is cited by the Office describes connection to a chip (566) rather than a corresponding signal trace. (See Col. 20, lines 54-56) Withdrawal of the rejection of claim 12 is therefore requested. Claims 29-33 are dependent claims which further distinguish the invention, and which are allowable for the same reason as claim 12. Withdrawal of the rejections of claims 29-33 is therefore requested.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Applicants' Attorney at 978-264-4001 (x305) so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application, including all claims currently under examination, is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

July 7, 2005
Date

Holmes W. Anderson, Reg. No. 37,272
Attorney/Agent for Applicant(s)
Steubing McGuinness & Manaras LLP
125 Nagog Park
Acton, MA 01720
(978) 264-6664

Docket No. 13888ROUS02U 120-042
dd: 06/07/2005